REMARKS

Claims 1-35 are pending. Claims 1, 3, 5, 6, 8, 19, 21, 22, 24, and 25 have been amended.

The Examiner's courtesy in conducting an interview with applicant's representative is acknowledged with appreciation. During the interview, the objection to the drawings was discussed. The Examiner indicated her view that the conductors and conductive traces are not shown in the Figures, and suggested that the term "signal lines" be used in their place. Applicant's representative maintained that conductors and conductive traces are shown in the Figures, as discussed further below. No agreement was reached.

The drawings have been objected to on the basis that "conductors" and conductive "traces" are not shown as recited in the claims. Applicant respectfully disagrees, and notes that signal lines B0, B1, B2, B3, and ground shields 60, are shown in Figs. 4 and 5. A copy of Fig. 4, is attached for reference, and shows signal lines B0, B1, B2, B3 (highlighted in yellow), and ground shields 60 (highlighted in orange), connecting between circuit element 58 and respective connector pins 62. The signal lines and ground shield are described in specification paragraph 0008, as follows:

> As shown in Fig. 3, the signal lines B0, B1 and B2 (three-bits of bus B) are looped through a connector 52, circuit card 54 and then back out on a different pin on the same connector 52 similarly as illustrated in Fig. 2. A ground shield 60 is provided on each side of the signal lines (only illustrated on each side of B1 in Fig. 3 for clarity). The shield 60 provides a coupling path from the signal line B1 to ground, as opposed to the adjacent signal lines B0 and B2.

The paragraph above reveals that Applicant's specification distinguishes between signal lines B0, B1, B2and ground shields 60. Further, claims 1 and 19 as originally filed recited "a plurality of conductors." Similarly, claims 8, 15, and 30 as originally

filed recited a "plurality of conductive traces to conduct signals." Thus, the present specification uses the terms 'signal traces' and 'conductive traces' to refer to conductors that carry signals. The term 'conductors' is used more generally to refer to signal traces, conductive traces, and ground shield. The terms conductors, ground shields, signal traces, and conductive traces were described, shown, and claimed in the application as originally filed. Withdrawal of the objection to the drawings is requested.

Claims 1-2, 5-9, 11-12, 14-16, 18-21, 24, 26-27, 29-31, and 33-34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,658,530 to Robertson et al. This rejection is traversed.

Claim 1 recites a circuit card including "a circuit element having a plurality of inputs and a plurality of outputs," and "a connector having a plurality of pins." The circuit card also includes "a plurality of conductors," each of the "conductors being coupled respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said pins." The plurality of conductors has "a first portion for conducting bus signals and a second portion for providing a shield," with the "conductors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors."

Robertson et al. discloses a circuit card (PCB 101) having a plurality of signal traces. The signal traces are connected to signal pins. Most signal pins are located directly adjacent to a ground pin. The ground pins are connected to a ground plane of PCB 101. See col. 3, lines 60-62. Robertson et al. postulates that the ground pins might improve signal integrity by reducing crosstalk between signal pins. Robertson et al. does not teach or suggest a circuit card having a plurality of conductors, each of the

conductors coupled between circuit element inputs, or circuit element outputs, and respective circuit card pins, in which the plurality of conductors has "a first portion for conducting bus signals and a second portion for providing a shield." Instead, Robertson et al. discloses only that signal lines connected between a circuit element to signal line pins, whereas the ground pins are connected to a *ground plane.*[1] Further, Robertson et al. does not teach or suggest that the conductors in the first portion are "grouped in a plurality of corresponding pairs," with "a respective one of said conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors." Instead, Robertson et al. discloses only that ground *pins* may reduce crosstalk between signal line *pins.*, and provides no teaching or suggestion of conductors of said second portion (shields) being located on each side of the signal conductors. Claim 1 is patentable over Robertson et al. Claims 2-5 depend from claim 1, and are patentable for at least the same reasons.

Claim 6 recites a circuit card having a connector with a plurality of pins, and a plurality of conductors coupled at a first end respectively to one of the plurality of pins. A circuit element has "a plurality of inputs and a plurality of outputs." The conductors are coupled "at a second end respectively to one of said plurality of inputs or one of said plurality of outputs." A first portion for the conductors conducts "bus signals," and a second portion provides "a shield." Conductors in the first portion are "grouped in a plurality of corresponding pairs." A respective one of the conductors in the second portion is located "on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors."

[1] During the interview, the Examiner argued that Robertson et al. "inherently" includes conductors connecting the ground pins to the circuit element. The disclosure in Robertson et al. that the ground pins are connected to a ground plane contradicts this.

Robertson et al. does not disclose any structure or arrangement of conductors such as that recited in claim 6 of the present application. The device disclosed by Robertson et al. features ground pins connected to a ground plane. Robertson et al. does not disclose a second portion of a plurality of conductors coupled at a first end respectively to one of a plurality of pins, and at a second end respectively to one of a plurality of inputs or one of a plurality of outputs, to provide a shield. Instead, according to Robertson et al., the ground *pins* reduce crosstalk between signal *pins*. Further, signal *lines* that connect between pins and a circuit element are not "grouped in a plurality of corresponding pairs," with a respective one of the conductors in the second portion of conductors providing a shield being located "on each side of each of said plurality of corresponding pairs of said first portion of said plurality of conductors." Claim 6 is patentable over Robertson et al. Claim 7 is dependent on claim 6, and is patentable for at least the same reasons.

Claim 8 recites a circuit card comprising "a first plurality of conductive traces connecting between contact pins and a an integrated circuit element to conduct signals, said first plurality of conductive traces being grouped in a plurality of corresponding pairs." The circuit card also comprises "a second plurality of conductive traces extending adjacent said first plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located on each side of each of said plurality of corresponding pairs of said first plurality of conductive traces."

Robertson et al. does not disclose the arrangement of conductors recited in claim 8. Claim 8 is patentable over Robertson et al. Claims 9 and 10 depend from claim 8, and are patentable for at least the same reasons.

Claim 11 recites a memory expansion card comprising "a memory device having a plurality of inputs and outputs," "a connector having a plurality of pins," and

"a plurality of traces." Each of the plurality of inputs and outputs of the memory device is "coupled by a respective trace to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector." A first portion of the plurality of traces is for "conducting signals" and a second portion of the plurality of traces for "providing a shield." The traces in the first portion are grouped "in a plurality of corresponding pairs." A respective one of the traces in said second (shield) portion is located "on each side of each of said plurality of corresponding pairs of said first portion of said plurality of traces." The first portion of the plurality of traces is part of a bus system.

Robertson et al. discloses a card with ground pins connected to a ground plane. Robertson et al. does not teach traces "providing a shield" located on each side of traces for conducting signals. Claim 11 is patentable over Robertson et al. Claims 12-14 depend from claim 11, and are patentable for the same reasons.

Claim 15 recites a memory expansion card comprising "a memory device having a plurality of inputs and a plurality of outputs," "a first plurality of conductive traces to conduct signals to said plurality of inputs or from said plurality of outputs, said first plurality of conductive traces being grouped in a plurality of corresponding pairs," and "a second plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces." The first plurality of conductive traces are part of a bus system.

Robertson et al. does not disclose a memory expansion card which includes "a first plurality of conductive traces to conduct signals to said plurality of inputs or from said plurality of outputs, said first plurality of conductive traces being grouped in a plurality of corresponding pairs," and a second plurality of conductive traces providing a shield, with "a respective one of said second plurality of conductive traces

being located to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces." Claim 15 is patentable over Robertson et al. Claims 16 and 17 depend from claim 15, and are patentable for at least the same reasons.

Claim 19 recites a memory expansion card comprising "a connector having a plurality of pins, said plurality of pins having a first portion for conducting signals and a second portion for providing a shield." The pins in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins." A plurality of conductive traces is "connected respectively to each of said pins, a portion of said conductive traces being connected respectively to said pins in said second portion and extending respectively along each side of conductive traces connected to said first portion of pins.". The first portion of pins is part of a bus system.

Robertson et al. does not disclose a memory expansion card with pins including first and second portions, with a plurality of conductive traces "connected respectively to each of said pins, a portion of said conductive traces being connected respectively to said pins in said second portion and extending respectively along each side of conductive traces connected to said first portion of pins." Claim 18 is patentable over Robertson et al.

Claim 19 recites a processing unit having a circuit card as recited in claim 1, and is patentable over Robertson et al. for the same reasons. Claims 20-25 depend from claim 19, and are patentable for at least the same reasons as claim 19.

Claim 26 recites a processing system having a memory expansion card as recited in claim 11, and is patentable over Robertson et al. for the same reasons. Claims

27-29 depend from claim 26, and are patentable for at least the same reasons as claim 26.

Claim 30 recites a processing system having a memory expansion card as recited in claim 15, and is patentable over Robertson et al. for the same reasons. Claims 31 and 32 depend from claim 30, and are patentable for at least the same reasons as claim 30.

Claim 33 recites a method of constructing a circuit card comprising steps of "providing a first plurality of pins on a connector of said circuit card, said first plurality of pins for conducting bus signals," "grouping said first plurality of pins into a plurality of corresponding pairs," and "providing a second plurality of pins on said connector of said circuit card." The second plurality of pins is "connected to a respective conductive trace extending along each side of pairs of traces connected to each corresponding pair of said first plurality of pins for providing a signal shield."

Robertson et al. discloses a circuit card made by connecting ground pins to a ground plane. Robertson et al. does not teach manufacturing a circuit card by "providing a second plurality of pins on said connector of said circuit card," the second plurality of pins being "connected to a respective conductive trace extending along each side of pairs of traces connected to each corresponding pair of said first plurality of pins for providing a signal shield." Claim 33 is patentable over Robertson et al. Claims 34 and 35 depend from claim 33 and are patentable for at least the same reasons.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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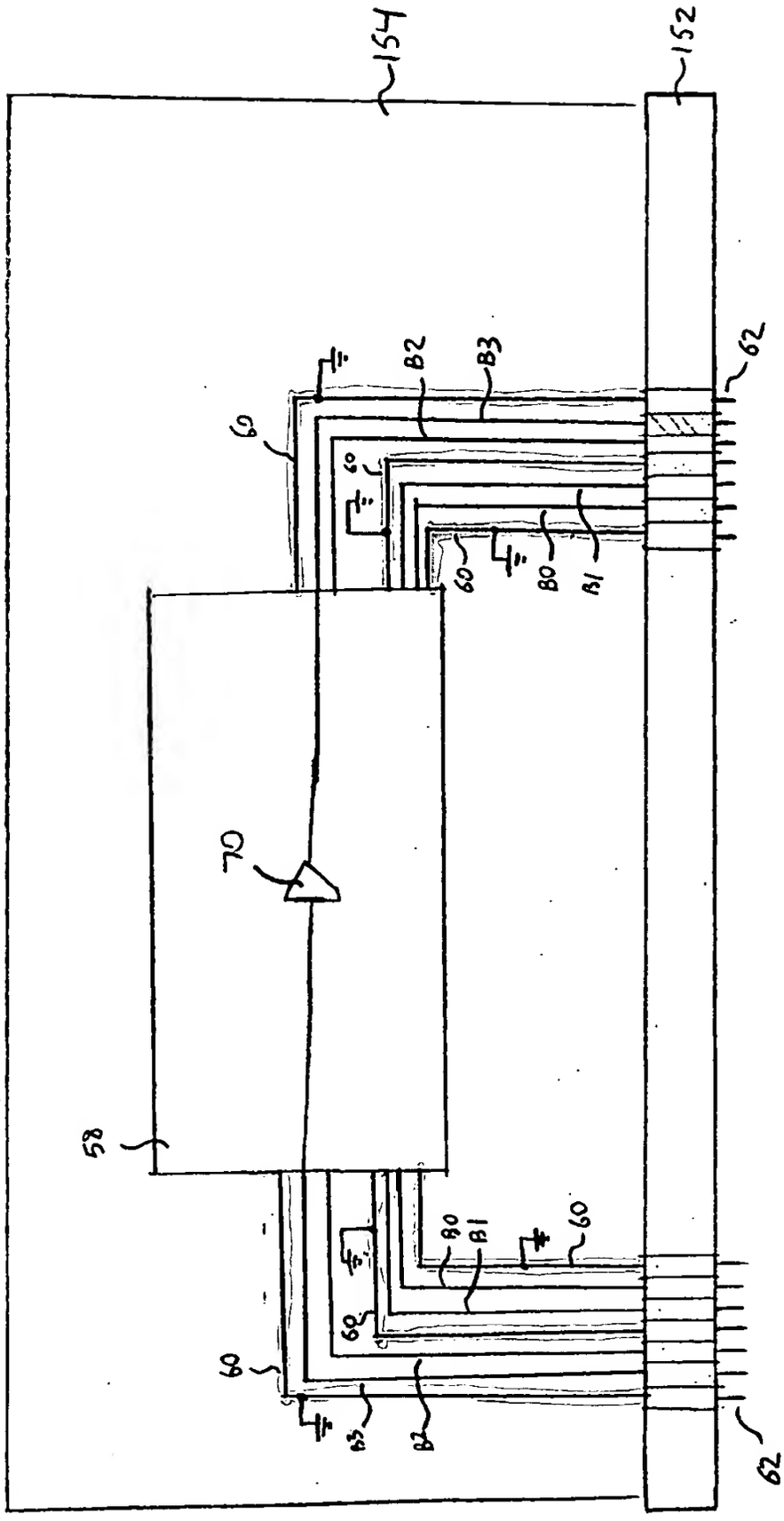

FIG. 4